in the following sections. Consideration of all amendments is politely requested.

AMENDMENTS TO THE CLAIMS

Claim 1 (currently amended): A method of fabricating a metal-oxide semiconductor transistor (MOS transistor) on a substrate comprising:

sequentially forming a gate oxide layer and a gate on the substrate;

performing a first ion implantation process to form a first doped region in the substrate;

sequentially forming a liner layer, a dielectric layer and a sacrificial layer on the substrate;

~~forming a L-shaped spacer on either side of the gate;~~

performing a first etching process to simultaneously form an arc-shaped spacer on either side of the gate and remove portions of the dielectric layer and the sacrificial layer atop the gate by utilizing the liner layer as a first stop layer;

performing a second etching process to remove portions of the sacrificial layer within the arc-shaped spacer by utilizes the dielectric layer as a second stop layer, and constructing a L-shaped spacer

on either side of the gate;

performing a third etching process to remove portions of the liner layer not covered by the L-shaped spacer;

performing a second ion implantation process to form a second doped region with a gradient profile in portions of the substrate adjacent to either side of the L-shaped spacer; and

performing a self-aligned silicide (salicide) process to form a silicide layer on the gate and on exposed portions of the substrate surface above the second doped region.

Claim 2 (original): The method of claim 1 wherein the substrate is a silicon substrate.

Claim 3 (original): The method of claim 1 wherein the gate comprises an offset spacer on either side of the gate.

Claim 4-5 (cancelled)

Claim 6 (currently amended): The method of claim [[5]]1 wherein the liner layer, the dielectric layer and the

sacrificial layer respectively comprise silicon oxide, nitride and polysilicon.

Claim 7 (cancelled)

Claim 8 (original): The method of claim 1 wherein the first and second doped regions are in a gradient profile, the first doped region is employed as a source/drain extension, and the second doped region comprises a step source/drain extension and a source/drain of the MOS transistor employed to prevent leakage current of the silicide layer.

Claim 9 (original): The method of claim 8 wherein the depth and the width of the step source/drain extension are respectively determined by the thickness of the dielectric layer and the width of the L-shaped spacer.

Claim 10 (original): The method of claim 8 wherein the silicide layer is formed by the steps of:

forming a metal layer on the gate and on portions of the substrate surface above the source/drain;

performing a first rapid thermal process (RTP);

performing a wet etching process to remove

unreacted portions of the metal layer on the surface of the substrate; and

performing a second RTP.

Claim 11 (original): The method of claim 10 wherein the metal layer comprises cobalt (Co).

Claim 12 (original): The method of claim 1 wherein the first and second doped regions are doped with either arsenic (As) atoms or phosphorus (P) atoms.

Claim 13 (original): The method of claim 1 wherein the first and second doped regions are doped with either one of boron difluoride (BF_2^+) ions, boron (B) atoms or indium (In) atoms.

Claim 14 (currently amended): A method of fabricating a MOS transistor on a substrate comprising:

sequentially forming a gate oxide layer and a gate on the substrate;

performing a first ion implantation process to form a first doped region in the substrate;

forming a liner layer to cover the substrate;

sequentially forming a dielectric layer and a

sacrificial layer on the liner layer;

~~forming a L-shaped spacer on either side of the gate;~~

~~performing a first etching process to remove portions of the liner layer not covered by the L-shaped spacer;~~

performing a first etching process to simultaneously form an arc-shaped spacer on either side of the gate and remove portions of the dielectric layer and the sacrificial layer atop the gate by utilizing the liner layer as a first stop layer;

performing a second etching process to remove portions of the sacrificial layer within the arc-shaped spacer by utilizes the dielectric layer as a second stop layer, and constructing a L-shaped spacer on either side of the gate;

performing a third etching process to remove portions of the liner layer not covered by the L-shaped spacer;

performing a second ion implantation process to simultaneously form a second doped region and a third doped region in the substrate; and

performing a salicide process to form a silicide layer on the gate and on portions of the substrate

surface above the third doped region.

Claim 15 (original): The method of claim 14 wherein the substrate is a silicon substrate.

Claim 16 (original): The method of claim 14 wherein the first, second and third doped regions are in a gradient profile and are respectively employed as a source/drain extension, a step source/drain extension and a source/drain of the MOS transistor, and the second doped region is employed to prevent leakage current of the silicide layer.

Claim 17 (original): The method of claim 14 wherein the liner layer, the dielectric layer and the sacrificial layer respectively comprise silicon oxide, nitride and polysilicon.

Claim 18-19 (cancelled)

Claim 20 (original): The method of claim 14 wherein the first, second and third doped regions are doped with either arsenic atoms or phosphorus atoms.

Claim 21 (original): The method of claim 14 wherein the first, second and third doped regions are doped with either one of boron difluoride ions, boron atoms or indium atoms.

Claim 22 (original): The method of claim 14 wherein the depth and the width of the second doped region are respectively determined by the thickness of the dielectric layer and the width of the L-shaped spacer.

Claim 23 (original): The method of claim 14 wherein the silicide layer is formed by the steps of:

forming a metal layer on the gate and on portions of the substrate surface above the third doped region;

performing a first RTP;

performing a wet etching process to remove unreacted portions of the metal layer on the surface of the substrate; and

performing a second RTP.

Claim 24 (original): The method of claim 23 wherein the metal layer comprises cobalt.

REMARKS

Claims 1-5, 7-9, 14-16 and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Yu (US 6,506,650). Claims 6, 10-13, 17-21 and 23-24 are rejected under 35 U.S.C 103(a) as being unpatentable over Yu (US 6,506,650) in further view of Lee et al. (US 5,153,145).

1. Response to the rejection of claims 1-5, 7-9, 14-16 and 22 under 35 U.S.C. 102(e):

Claims 1, 6 and 14 are amended to distinctly distinguish the characteristics of this application. No new matter has been introduced, and the amended claims are fully supported by the specification and figures as filed.

In this application, a method of fabricating a MOS transistor is disclosed. Although the cross-sectional profile of this application is similar to that of US 6,506,650, **the method of forming a L-shaped spacer is different.**

In this application, for fabricating a L-shaped spacer, firstly etching **the dielectric layer and the**

sacrificial layer to form an arc-shaped spacer, and then etching **the sacrificial layer within the arc-shaped spacer** to form a L-shaped spacer. Finally, etching **the liner layer** not covered by the L-shaped spacer.

In US 6,506,650, for fabricating a L-shaped spacer, the sacrificial layer is firstly etched to form an arc-shaped mask, and then the dielectric layer and the liner layer are etched simultaneously to form a L-shaped spacer. Finally, the arc-shaped sacrificial layer is removed. (US 6,506,650 col. 1 line 66-col. 2 line 15, col. 3 lines 32-49)

The fabricating processes of these two inventions are definitely different. Features in the amended independent claims 1 and 14 are novel and never disclosed, so consideration of the claims 1-5, 7-9, 14-16 and 22 is therefore politely requested.

2. Response to the rejection of claims 6, 10-13, 17-21 and 23-24 under 35 U.S.C. 103(a):

According to the statement of the **MPEP Sec. 2143.03**, which is repeated as follows:

"If an independent claim is non-obvious under 35

U.S.C. 103, then any claim depending therefrom is non-obvious." (In re Fine, 837 F.2d 1071, 5 USPQ(CCPA 1988))

Claims 6 and 10-13 are dependent on amended claim 1 and should be allowed if the amended claim 1 is allowed. Claims 17-21 and 23-24 are dependent on amended claim 14 and should be allowed if the amended claim 14 is allowed. Reconsideration of the rejection of claims 6, 10-13, 17-21 and 23-24 is therefore politely requested.

Sincerely yours,

Winston Hsu

Date: 9/17/2003

Winston Hsu, Patent Agent No.41,526
P.O. BOX 506
Merrifield, VA 22116
U.S.A.
e-mail: winstonhsu@naipo.com.tw